EMBEDDED SYSTEM DEVELOPMENT FOR TSUNMI DETECTION

A thesis submitted in the partial fulfilment of the requirements for the degree of

Bachelor of Technology
In
Electronics & Instrumentation Engineering

Submitted by:

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Under the guidance of
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CERTIFICATE

This is to certify that the thesis entitled "Embedded system development for Tsunami detection" submitted by **PRIYABRAT PARHI**, Final year student of Electronics & Instrumentation Engineering, Roll No: 109EI0056 and **PRABHUPAD BHOI**, Final year student of Electronics & Instrumentation Engineering, Roll No: 109EI0262 in partial fulfilment of the requirements for the award of B.Tech degree at NATIONAL INSTITUTE OF TECHNOLOGY, ROURKELA is a project work carried out by them under my supervision.

To the best of my knowledge, the matter embodied in the thesis has not been submitted to any other university/institute for the award of any degree or diploma.

DATE:

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An assemblage of this nature could never have been attempted without reference to and inspiration from the works of others whose details are mentioned in the reference section. We acknowledge our indebtedness to all of them.

Last but not the least our sincere thanks to all our friends, who have patiently extended all sorts of help for accomplishing this undertaking.

ABSTRACT

In this project, we present the implementation of a low cost prototype of a Tsunami detection system to detect the occurrences of tsunami, at significantly smaller laboratory scale. The implementation of the system is based on the principle of vary in water pressure and temperature at the time of occurrence of Tsunami. In this paper we includes the experimentally recorded response from the Spartan 3E FPGA board and the microcontroller giving an indication as well as a prediction of water pressure at remote place for the detection of water turbulence similar to the case of tsunami. It has been found that the system developed works very well in the laboratory scale.

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CONTENTS

CHAPTER-1

INTRODUCTION

In recent years there is an increasing interest on the development of sensor based instrumentation systems suitable for the detection of tsunami. It is a known fact that, early detection of tsunami enables us to take the necessary preventive steps to avoid the possible disaster and loss of life. Tsunami is known to be generated by any disturbance that displaces a large mass of water. Studies on the cause, nature and detection of tsunami waves allow us to infer that they are indeed a dynamic phenomenon, which can only be detected or measured with respect to pressure and temperature changes associated with the waves. In the present paper, we report the study and implementation of a pressure sensor based low-cost system to detect the occurrences of tsunami at significantly smaller laboratory scale. The advantage of using an embedded system for developing a Tsunami warning system is its accuracy and speed and also it uses capacitive sensors which are highly sensitive even for a small level pressure changes. Moreover, this system has very long life and it is cheaper than the existing system.

Generation of Tsunami

A Tsunami is a very long-wavelength wave of water that is generated by earthquakes that cause displacement of the seafloor, but Tsunami can also be generated by volcanic eruptions, landslides and underwater explosions that causes displacement of water column vertically upward. Tsunami occur suddenly, often without warning, they are extremely dangerous to the coastal communities. Tsunami earthquakes however, are a rare class of earthquakes that rupture more slowly at 1-1.5 km per second and propagate up to the sea floor. This makes the vertical uplift much larger resulting wave heights up to 10-20 metres.

What is is tsunami detection system?

Deep ocean tsunami detection buoys are one of the two types of instrument used by the Bureau of Meteorology to confirm the existence of tsunami waves generated by undersea earthquakes. These buoys observe and record changes in sea level in the deep ocean. This enhances the capability for early detection of tsunami and real-time reporting of danger before they reach land.

How does tsunami detection buoy work?

A typical tsunami buoy system comprises of two components; the pressure sensor anchored to the sea floor and the surface buoy. The sensor on the sea floor measures the change in height of the water column above by measuring associated changes in the water pressure. This water column height is communicated to the surface buoy by acoustic telemetry and then relayed via satellite to the nearest tsunami warning centre. The system has two modes of operation 'standard mode' and 'event mode'. The system generally operates in 'standard' mode, where it routinely collects sea level information and reports via satellite at relatively low frequency transmission intervals (i.e. every 15 minutes). This helps to conserve battery life and hence extend the deployment life. The tsunami buoy is triggered into 'event' mode when the pressure sensor first detects the faster moving seismic waves moving through the sea floor. It then commences reporting sea level information at one minute intervals to enable rapid verification of the possible existence of a tsunami. The system returns to ‘standard mode’ after 4 hours if no further seismic events are detected.

How is the location for deployment of a tsunami buoy determined?

The best location for deployment of a tsunami buoy is determined by careful consideration of a number of factors. The tsunami buoy needs to be far enough away from any potential earthquake epicentre to ensure there is no interference between the earthquake signal at the buoy and the sea-level signal from the tsunami. On the other hand, the tsunami buoy needs to be close enough to the epicentre to enable timely detection of any tsunami and maximise the lead time of tsunami forecasts for coastal areas. In addition, tsunami buoys must ideally be placed in water deeper than 3000m to ensure the observed signal is not contaminated by other types of waves that have shallower effects (e.g. surface wind-waves). International maritime boundaries must also be considered when deploying tsunami buoy systems.

Tsunami detection system specification:-

The device used to collect the measurements has to be chosen between those equipped with sensors capable of detecting sea-level oscillations within the tsunami frequency band. At present, the main devices that can be actually be used should be:

I) Water pressure detecting sensor

ii) Transmitter Receiver circuit to get the water height at local area

iii) Intelligent embedded system to convert the analog signal to digital and apply the Tsunami detection algorithm.

CHAPTER-2

TSUNAMI DETECTION USING MICROCONTROLLER:-

Keywords:-

Cross Compiler, Embedded System, Microcontroller, Sensors, Transmitter,Buzzer.

System Architecture of Tsunami detection system:-

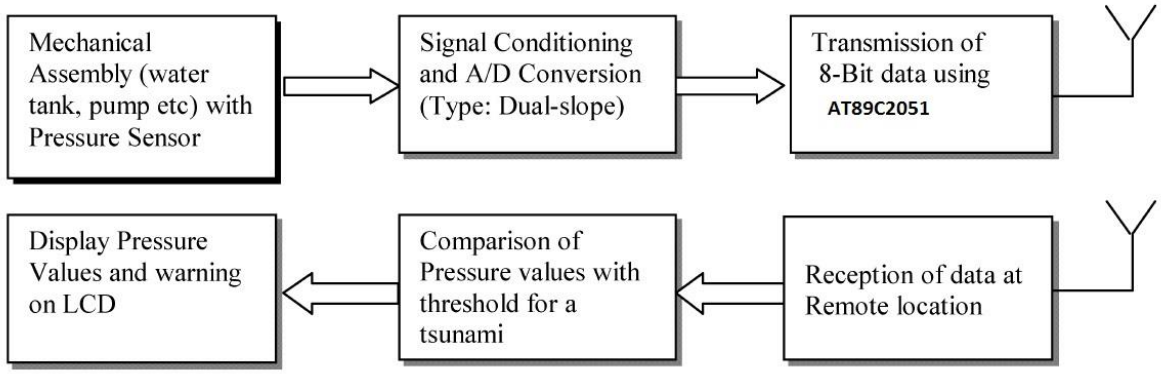


Figure 1. Block Diagram of the Tsunami Detection System

A block diagram of the system developed in our present study is shown in Fig. 1. It includes a mechanical assembly consisting of a water tank, pressure sensors and water pump with water pipe line & valve to simulate the turbulence and pressure variations similar to the case of tsunami. The system is used to carry out laboratory level Experimental studies. Inside the tank, suitable mountings are provided for the convenience of fixing the pressure sensors at different depths in water. The valve fixed in the water pipeline enables to control the water flow rate and hence the water pressure variations inside the tank. In order to have redundancy, two similar pressure sensors have been used and these were hermetically sealed.

Implementation:-

Capacitive pressure Sensor:-

Metal diaphragm type capacitive sensor is used in this study. This sensor contains a dielectric material separated by a metal diaphragm and an electric plate and comparator. When there is any variation in capacitance value, the comparator compares the actual value with the target value. Based on this principle, capacitive sensor gets operated.

Transmitter:-

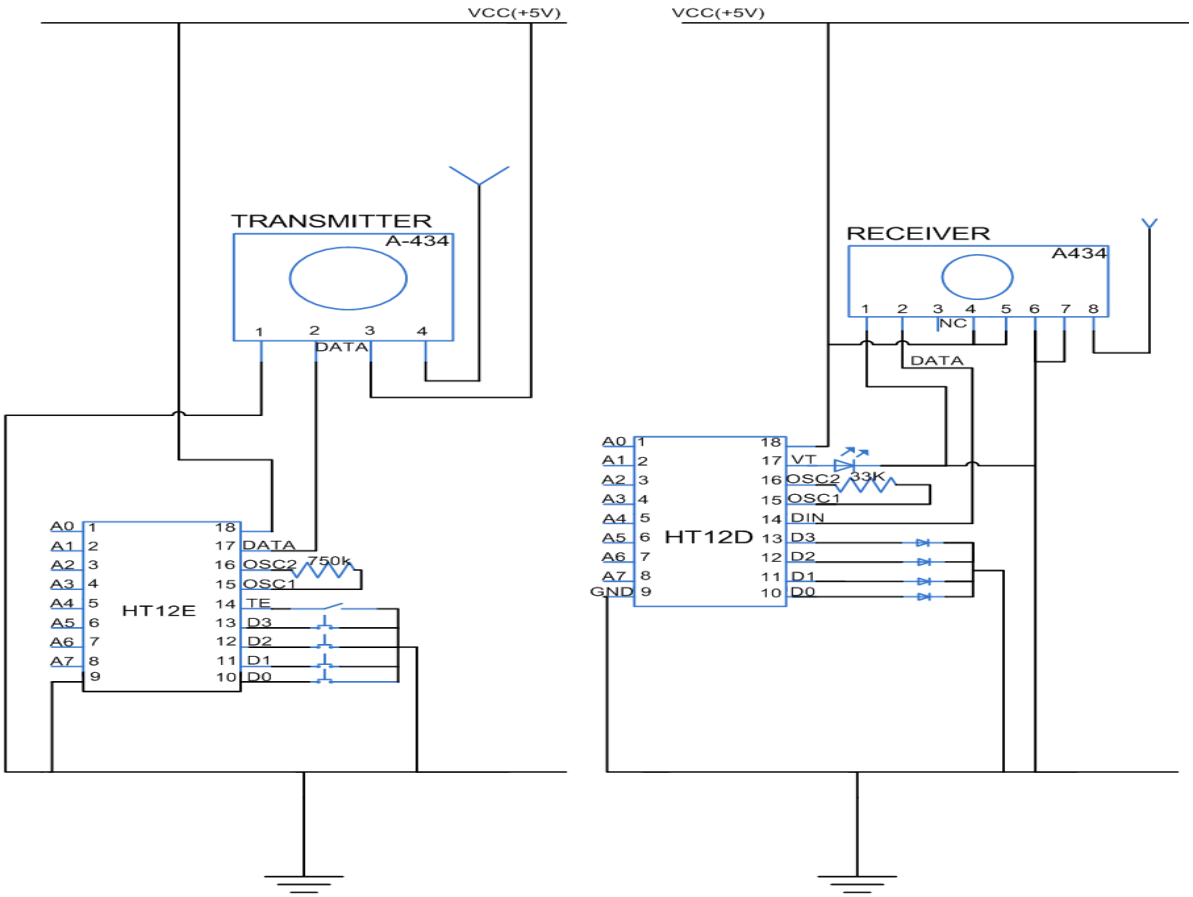
The RF transmitter is chosen because there is less noise and can be used for significantly large distances. In the transmitter module, the capacitive sensor senses the change in capacitance. This change in capacitance is sensed as an analog output voltage. This analog signal is then converted into digital signal by using ADC and the digital signal is fed to input port of microcontroller. Microcontroller compares the actual value with some threshold value. If the actual value exceeds the target value then it is considered as an abnormal condition. The value is given as interrupt signal to the AT89C2051 microcontroller. Then the data signal and carrier signal are generated by the microcontroller. Data signal is pulse code modulated with the carrier wave to transmit the analog signal. Negative pulse code modulation is performed. The signal is passed to receiver in the form of IR rays with the help of LED.

Receiver:-

RF receiver is used in this study which has the capability to receive frequency with the range of 38 kHz. TSOP 1738 is the standard IR remote control receiver series, supporting

all major transmission codes. The receiver module diagram is shown in figure 2. In the receiver module, TSOP1738 receives the signal in the input pin. This is given as input to another microcontroller. The PC is interfaced with the microcontroller through MAX-232 level converter, in order to convert TTL logic to RS logic. In MAX-232 11th pin takes the microcontroller TTL logic and process it and then gives the RS logic output on the 14th pin. The buzzer is interfaced with the microcontroller on the port P1.5.

The system allows one way communication between two nodes, namely, transmission and reception. The RF module has been used in conjunction with a set of four channel encoder/decoder ICs. Here HT12E & HT12D have been used as encoder and decoder respectively. The encoder converts the parallel inputs (from the remote switches) into serial set of signals. These signals are serially transferred through RF to the reception point. The decoder is used after the RF receiver to decode the serial format and retrieve the original signals as outputs. These outputs can be observed on corresponding LEDs.



(Circuit Diagram of RF module)

MAX-232 Level Converter:-

The MAX-232 level converter is a 16 pin DIP. It contains dual charge pump DC-DC voltage converters, RS 232 drivers, RS 232 receivers and receiver and transmitter enable control inputs.

RS232:_

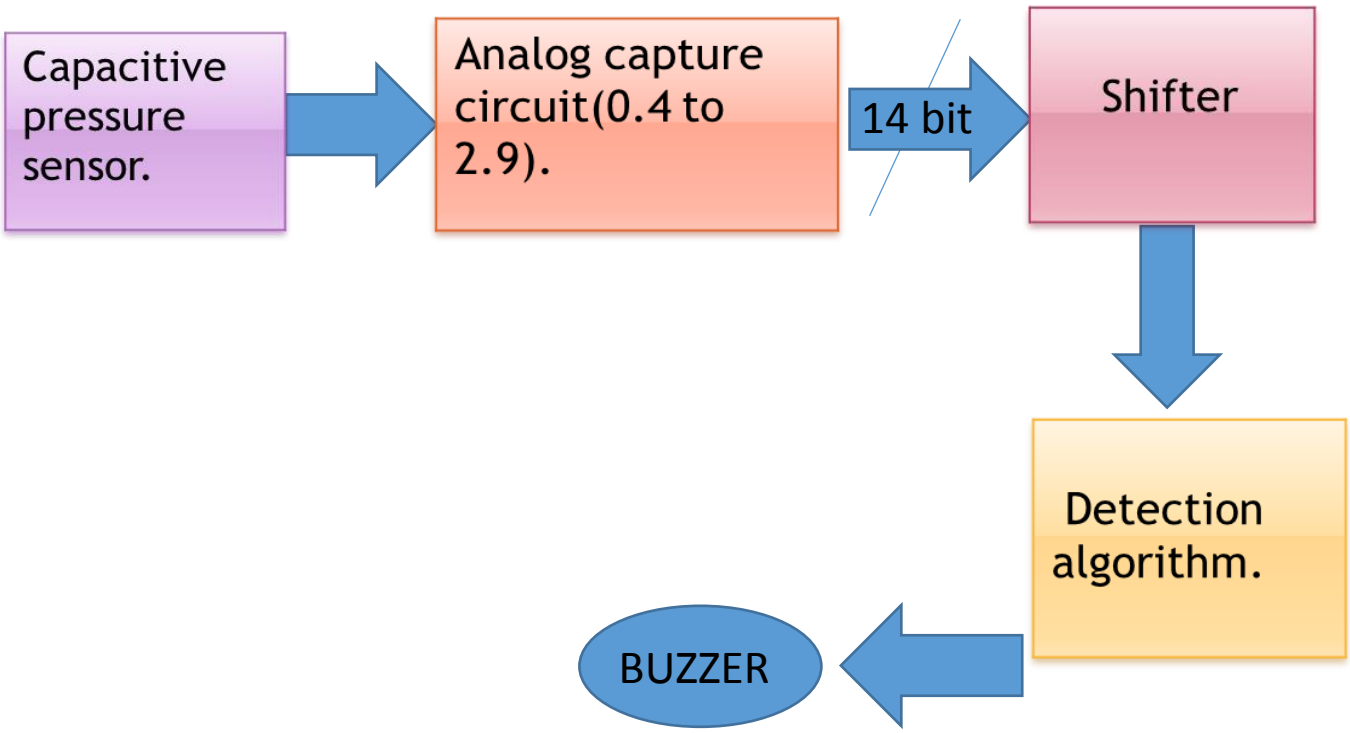
RS232 devices can be plugged straight into the computers serial port. This is referred to as COM port. The data acquisition device used here is capacitive sensors. Its output is fed through microcontroller. In warning phase mobile is connected to PC through the RS232 port.

In this semester we have basically implemented the RF module and the system using microcontroller (AT89C2051) which only gave the confirmation about the data communication and the microcontroller that whether the system is working well or not and because of that we have did a small operation on that by installing a simple program on the microcontroller.

CHAPTER- 3

Implementation using FPGA:-

Block Diagram:-



Algorithms for Automatic, Real-Time Tsunami Detection in Sea Level Measurements:-

In the case of BPRs, one very important requisite should also be considered and met. Owing to their location, these sensors must have an autonomous power supply. Therefore, the algorithm should run with the lowest possible power consumption. Such a requisite has not necessarily to be met by an algorithm implemented in the software of DART system located either on offshore platforms or elastic beacons, as well as tidal gauges, can actually be connected to a source of power by a cable. It is furthermore to be noticed that the characteristics of the algorithm may also depend on the apparatus for device to land data

transmission. As far as false alarm avoiding requisite is concerned, it should be noted that only filtering out non tsunami waves makes it possible to monitor the actual propagation of a tsunami by checking either the amplitude (amplitude-discriminating algorithm) or the slope (slope-discriminating algorithm) of the recorded signal against a prescribed threshold. Indeed, the presence of several frequencies in a sensor recorded signal guarantees the instrument's poly functionality. It is in-fact economically desirable to have a device that can measure the wider range of oscillation phenomena. While the 'disturbance' recorded by a BPR is caused by the superposition of actual sea-surface fluctuations (e.g. planetary waves, astronomical and meteorological tides, gravitational normal modes) and background sea noise , several other 'disturbances' may affect WWG measurements . In addition to the above listed wave patterns and to wind waves (for detecting which these sensors are designed), a near shore WWG can actually measure infra-gravity waves (e.g. bound/free-long waves, edge waves, surf beats).

It has been shown (Mofjeld, 1997; Beltrami, 2008) that the 'disturbance' recorded by a BPR can be closely predicted, making possible to filter it out simply by subtracting the values observed from those predicted. On the contrary, a close prediction of a wind-wave signal is not possible; therefore some form of low-pass digital filter has to be implemented in the tsunami detection algorithm of a WWG in order to filter out these waves. It is well known (e.g. Emery & Thomson, 2001), that an effective low-pass digital filter should possess five, often mutually exclusive, essential qualities:

1) A sharp cut-off, so that unwanted high-frequency components are effectively removed;

2) A comparatively flat pass-band that leaves the low frequencies unchanged;

3) A clean transient response so that rapid changes in the signal do not result in spurious oscillation or 'ringing' within the filtered record;

4) A zero phase shift; and

5) An acceptable computational time.

Another requisite should also be met in the context of automatic, real-time tsunami detection. The filter to be used should belong to the class of causal or physically realizable filters, i.e. to the class of filters that use as input only actually available or ’past’ signal samples. It is to be noticed that the use of only ’past’ samples makes a zero-phase response not possible for causal filters. A way to get round this problem is to design a filter that has, at least, a linear phase response, i.e. a symmetrical impulse response with location of symmetry shifted from the sample to be filtered. In fact, since this shift does nothing but produce an identical shift in the output signal, a linear phase filter is equivalent to a zero phase one for most purposes. It is finally to be stressed that, in the context of real-time tsunami detection, the time-domain approach to filter design undoubtedly possess the appealing pro of making the filtered signal immediately available.

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Detection in BPR measurements

The DART algorithm

The tsunami-detection algorithm developed by Mofjeld (1997) under the Deep-ocean Assessment and Reporting of Tsunami (DART) program uses a cubic polynomial to predict disturbing wave patterns. The filtered signal is obtained by subtracting at each new time step the prediction from the observation. The algorithm monitors the actual propagation of a tsunami by checking the amplitude of the filtered signal against a prescribed threshold (TSamp), and therefore belongs to the class of the amplitude-discriminating ones. The predictions ζp are updated every sampling interval (i.e. every 15 s), and the prediction time is set equal to 15 s in the future with respect to the actual time ti . The polynomial is fitted to p-

minute averages ζ (centred at the p/2 minute) of observations ζ collected over the preceding three hours and p minutes and can be expressed as

$$\zeta p(ti+1) = = \sum_{j=0}^{3} wj * \zeta(ti - 0.5p - 60j) \quad \text{----------} \quad (1)$$

where ti is the actual time expressed in minutes. The coefficients wj are calculated by applying the Newton's forward divided difference formula, using the preceding temporal parameters. And if we choose the value of wj as shown in the table then our prediction time will vary accordingly and the value of p is set to 10min so 0.5p gives us 5min that means the average height of the water wave at that 10min interval is equal to the water wave height at the 5th minute.

Coefficient	Prediction time 5.25 min	Prediction time 35.25 min
w0	+ 1.16818457031250	+2.45603613281250
w1	- 0.28197558593750	-2.72678027343750
w2	+ 0.14689746093750	+1.67295214843750
w3	- 0.03310644531250	-0.40220800781250

a) Regularize the polynomial fitting point pattern by filtering out background noise typically recorded by BPRs; and

b) minimize the extent to which an actually detected tsunami indirectly influences the filtered signal by affecting the observation averages .

As already stated, in this case (p=10 min) the prediction time is set equal to 15 s in the future with respect to the actual time ti , i.e. 5 minutes and 15 seconds in the future with respect to the time at which is centred the first average.

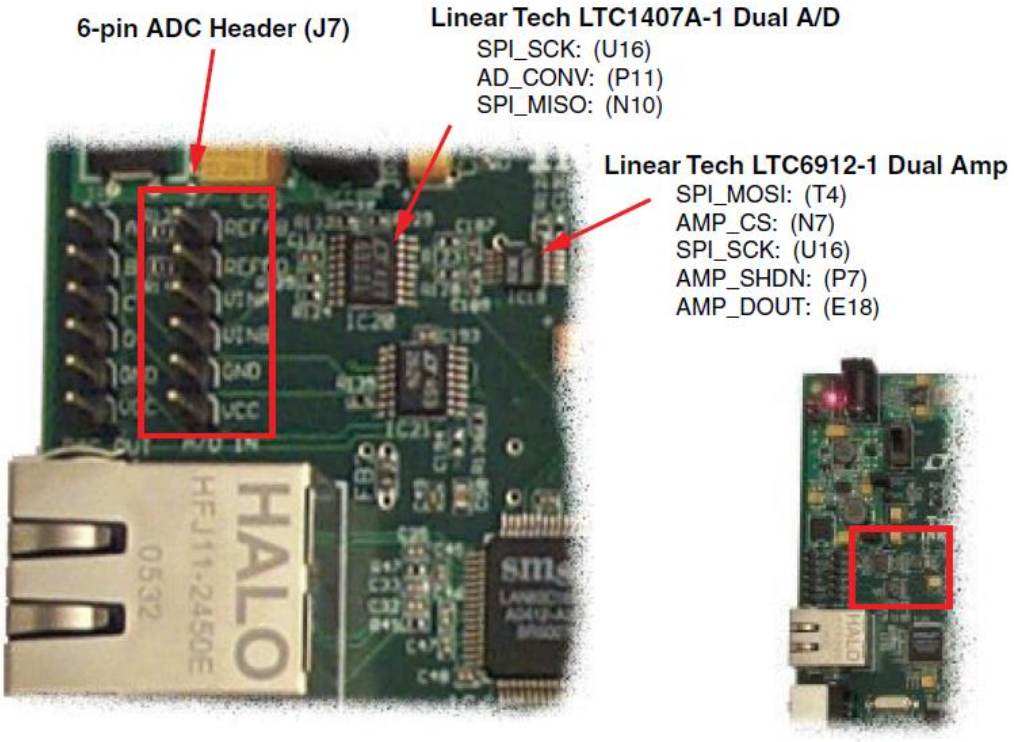
As shown by Beltrami , the algorithm's prediction error depends both on the time interval p and on the magnitude of the disturbance to be filtered out. In the absence of background sea-noise, this disturbance is mainly caused by the tide. Departure from a perfectly filtered signal (a zero signal) therefore depends on the measurement location. For example, the filtered signals obtained by testing the algorithm on M2 tides of equal phase and different amplitudes show a residual oscillation of sinusoidal shape. When p is equal to 10 min, the range of this oscillation (i.e. the prediction error) will be approximately 0.26 % of the tidal one. At a location that experiences a tidal range of 2.0 m, an oscillation with a range of 5.0 mm is therefore expected to persist in the filtered signal.

Whatever the time interval p, fixing all the preceding temporal parameters makes it possible to calculate the wj coefficients once and for all and a priori. The implementation of equation (1) is therefore particularly simple. Furthermore, the coefficients wj are calculated on the sole basis of temporal parameters. This makes the same set applicable to all BPRs, whatever their location. Such characteristics, together with a filtering performance that is effective from a practical point of view, constitute the algorithm's main strengths.

Implementation of the system on FPGA:-

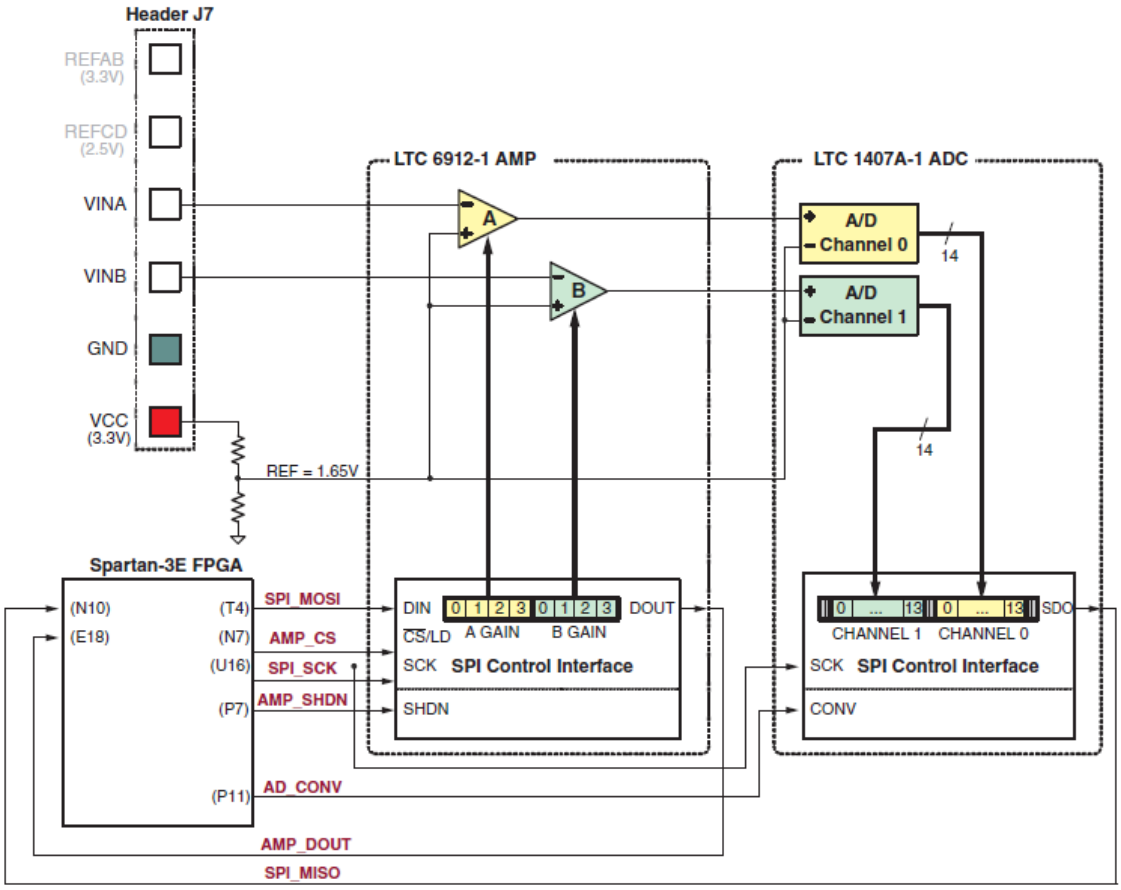
Analog capture circuit:-

The Spartan-3E FPGA Starter Kit board includes a two-channel Analog capture circuit, consisting of a programmable scaling pre-amplifier and an Analog-to-digital converter (ADC), as shown in the given figure. Analog inputs are supplied on the J7 header. The Analog capture circuit consists of a Linear Technology LTC6912-1 programmable preamplifier that scales the incoming analog signal on header J7 .The output of pre-amplifier connects to a Linear Technology LTC1407A-1 ADC. Both the pre-amplifier and the ADC are serially programmed or controlled by the FPGA.



Two-Channel Analog Capture Circuit

figure1.1



Detailed View of Analog Capture Circuit

figure1.2

Digital Outputs from Analog Inputs

The Analog capture circuit converts the Analog voltage on VINA or VINB and converts it to a 14-bit 2's complemented digital representation, D [13:0], as expressed by Equation(2)

$$Equation\ D[13:0] = GAIN * \frac{V_{in} - 1.65\text{v}}{1.25\ \text{v}} * 8192 \text{---------- (2)}$$

The GAIN is the current setting loaded into the programmable pre-amplifier. The various allowable settings for GAIN and allowable voltages applied to the VINA and VINB inputs appear in Table. The reference voltage for the amplifier and the ADC is 1.65V, generated via a voltage divider shown in Figure. Consequently, 1.65V is subtracted from the input voltage on VINA or VINB. The maximum range of the ADC is +/-1.25V, cantered around the reference voltage, 1.65V. Hence, 1.25V appears in the denominator to scale the analog input accordingly.

Finally, the ADC presents a 14-bit, two's complement digital output. A 14-bit, two's Complement number represents values between -2^13 and 2^13-1. Therefore, the quantity is scaled by 8192 or 2^13. See. To control the GAIN settings on the programmable pre-amplifier we adjust the 8-bit data byte A0 A1 A2 A3 B0 B1 B2 B3. The voltage applied on VINA or VINB to the J7 header is AC signal.

Programmable Pre-Amplifier:-

The LTC6912-1 provides two independent inverting amplifiers with programmable gain. The purpose of the amplifier is to scale the incoming voltage on VINA or VINB so that it maximizes the conversion range of the ADC, namely 1.65 +/-1.25V.

The given Table lists the interface signals between the FPGA and the amplifier. The SPI_MOSI, SPI_MISO, and SPI_SCK signals are shared with other devices on the SPI bus. The

AMP_CS signal is the active-Low slave select input to the amplifier maximizes the conversion range of the ADC, namely 1.65 +/-1.25V.

Signal	FPGA Pin	Direction	Description
SPI_MOSI	T4	FPGA_AD	Serial data: Master Output, Slave Input. Presents 8-bit programmable gain settings.
AMP_CS	N7	FPGA_AMP	Active-Low chip-select. The amplifier gain is set when signal returns High
SPI_SCK	U16	FPGA_AMP	Clock
AMP_SHDN	P7	FPGA_AMP	Active-High shutdown, reset
AMP_DOUT	E18	FPGA_AMP	Serial data. Echoes previous amplifier gain settings. Can be ignored in most applications.

Table-1

Programmable Gain:-

Each analog channel has an associated programmable gain amplifier. Analog signals presented on the VINA or VINB inputs on header J7 are amplified relative to 1.65V. The 1.65V reference is generated using a voltage divider of the 3.3V voltage supply.

GAIN	A3	A2	A1	A0	Input Voltage range	
	B3	B2	B1	B0	Minimum	maximum
0	0	0	0	0		
-1	0	0	0	1	0.4	2.9
02	0	0	1	0	1.025	2.275
-5	0	0	1	1	1.4	1.9
-10	0	1	0	0	1.525	1.712
-20	0	1	1	0	1.5875	1.675
-50	0	1	1	0	1.625	1.675
-100	0	1	1	1	1.6375	1.662

Table -2

SPI Control Interface:-

Figure 1-3 highlights the SPI-based communications interface with the amplifier. The gain for each amplifier is sent as an 8-bit command word, consisting of two 4-bit fields. The most-significant bit, B3, is sent first

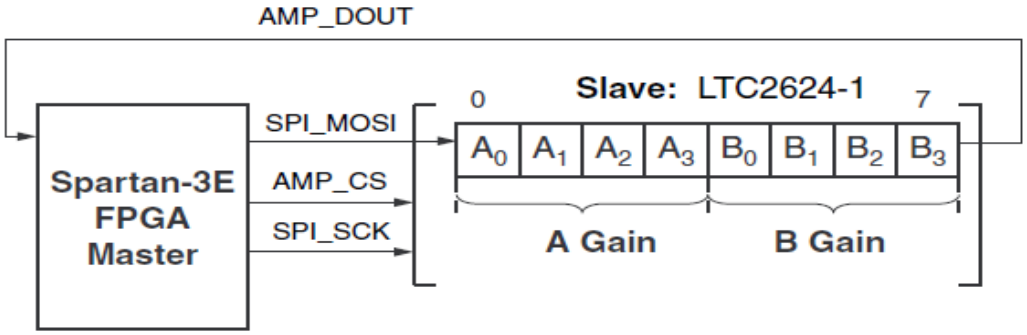


Figure **1-3 SPI Serial Interface to Amplifier**

The AMP_DOUT output from the amplifier echoes the previous gain settings. These values can be ignored for most applications. The SPI bus transaction starts when the FPGA asserts AMP_CS Low . The amplifier captures serial data on SPI_MOSI on the rising edge of the SPI_SCK clock signal. The amplifier presents serial data on AMP_DOUT on the falling edge of SPI_SCK.

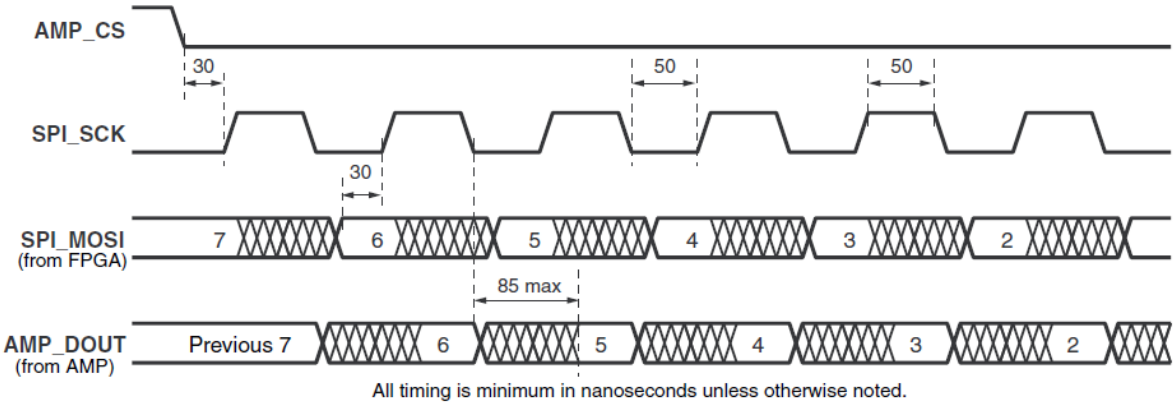


Figure 1 -4: **SPI Timing When Communicating with Amplifier**

The amplifier interface is relatively slow, supporting only about a 10 MHz clock frequency.

Analog to Digital Converter (ADC):-

The LTC1407A-1 provides two ADCs. Both analog inputs are sampled simultaneously when the AD_CONV signal is applied.

Interfacing

Table 1 lists the interface signals between the FPGA and the ADC. The SPI_MOSI, SPI_MISO, and SPI_SCK signals are shared with other devices on the SPI bus. The DAC_CS signal is the active-Low slave select input to the DAC. The DAC_CLR signal is the active-Low, asynchronous reset input to the DAC.

SPI Control Interface

Figure 1.6 provides an example SPI bus transaction to the ADC. When the AD_CONV signal goes high, the ADC simultaneously samples both analog channels. The results of this conversion are not presented until the next time AD_CONV is asserted, a latency of one sample. The maxim sample rate is approximately 1.5 MHz. The ADC presents the digital representation of the sampled analog values as a 14-bit, two's complement binary value.

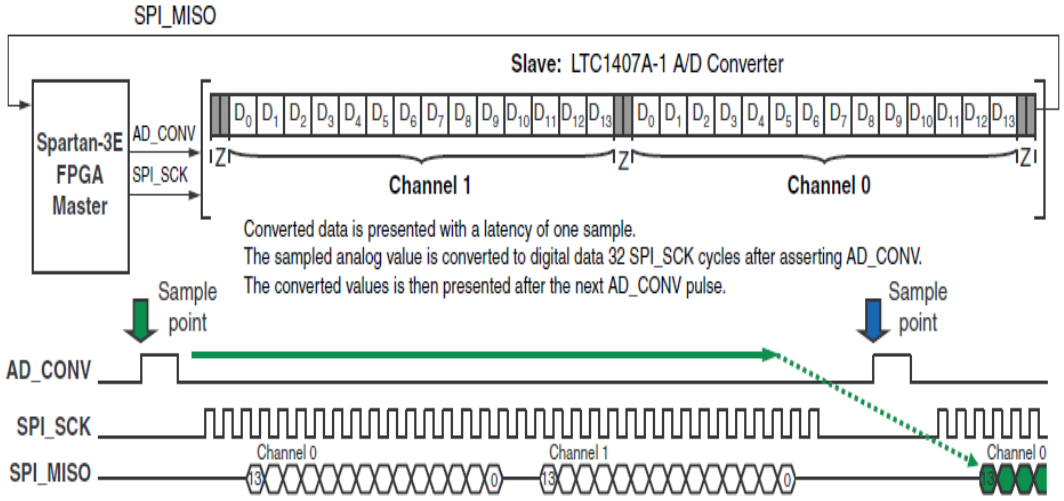


Figure 1 -6: **Analog-to-Digital Conversion Interface**

Figure 1-7 shows detailed transaction timing. The AD_CONV signal is not a traditional SPI slave select enable. Be sure to provide enough SPI_SCK clock cycles so that the ADC leaves

the SPI_MISO signal in the high-impedance state. Otherwise, the ADC blocks communication to the other SPI peripherals. As shown in Figure, use a 34-cycle communications sequence. The ADC 3-states its data output for two clock cycles before and after each 14-bit data transfer.

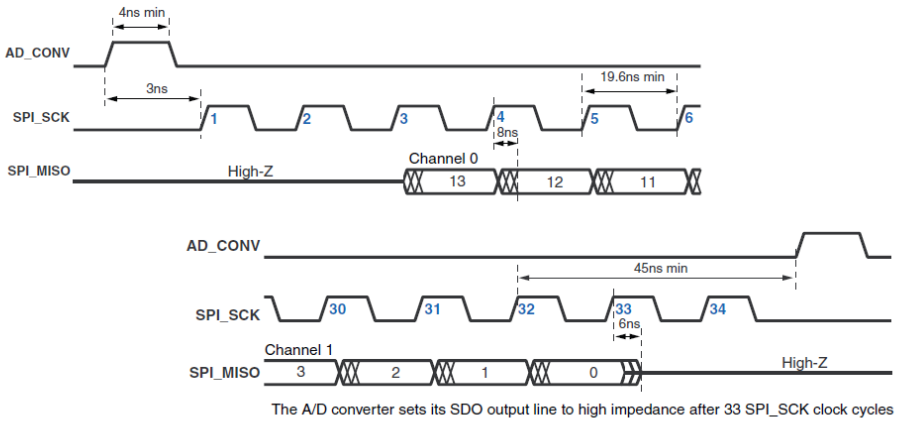
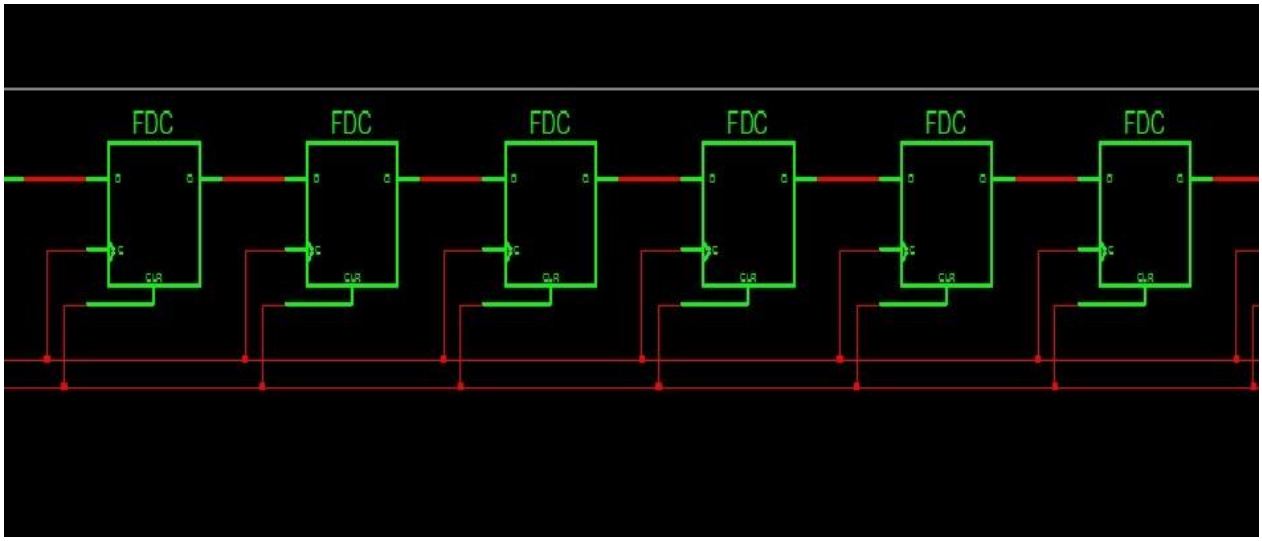


Figure 1 -7: **Detailed SPI Timing to ADC**

Connect AC signals to VINA or VINB via a DC blocking capacitor, and we get the 2's complemented 14 bit digital output at the required output location.

Saving on memory using shifter:-

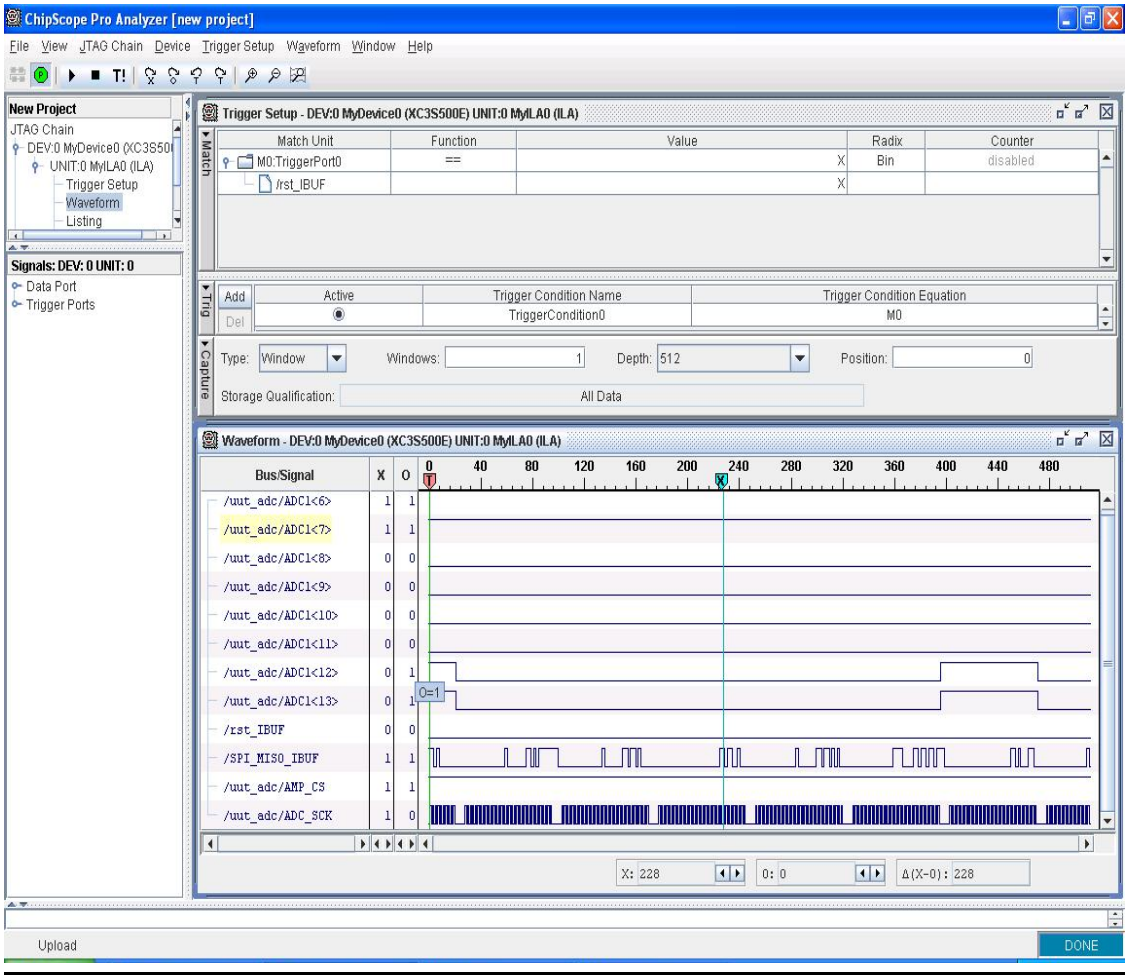
The 14 bit digital data received from the Analog capture circuit is saved on a memory array of 720 locations each of 14 bit . The RTL(register transistor logic) of the shifter is as shown below.



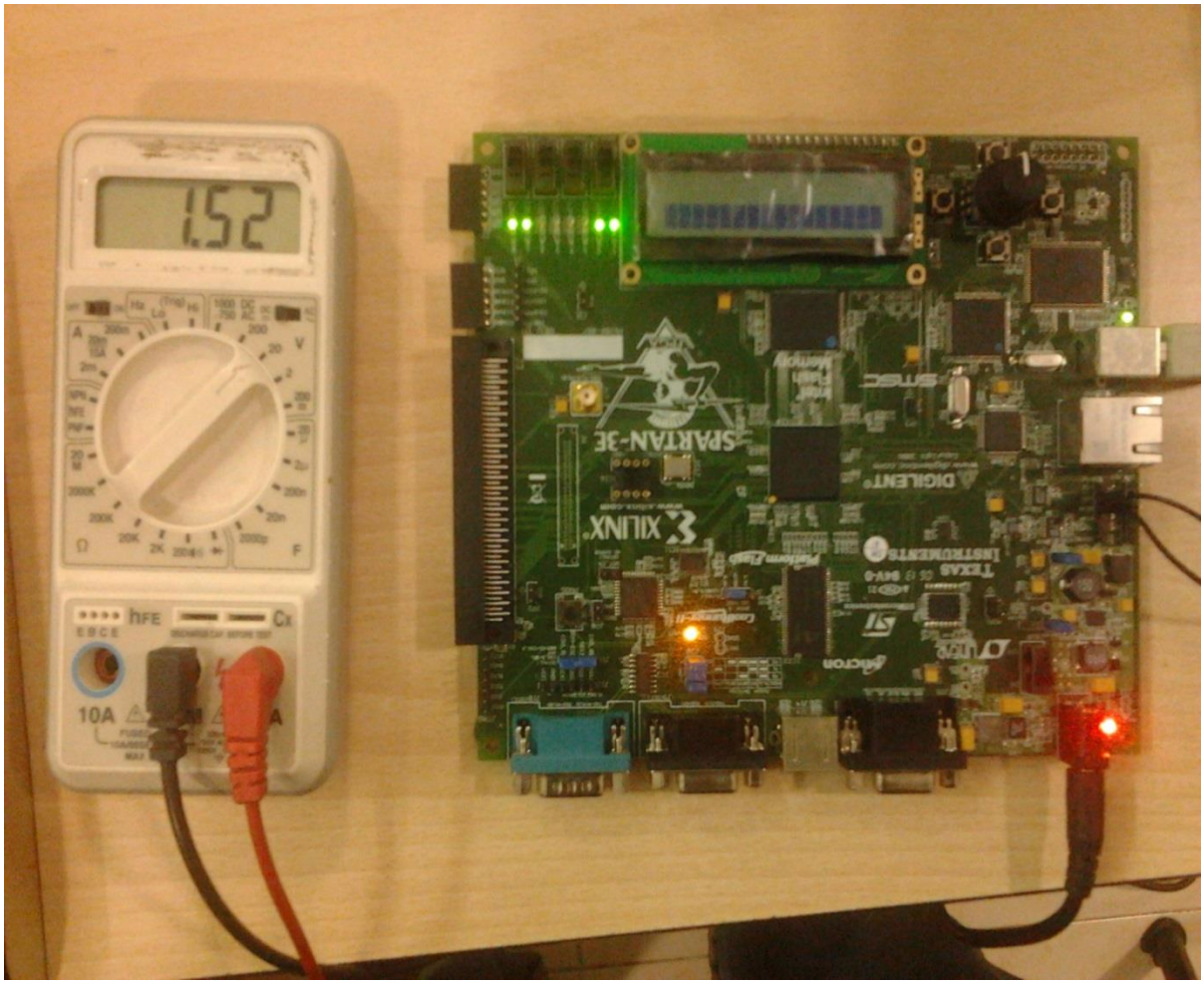
As shown in the figure the contains total 720 D-flip flops the data received from the ADC is shifted one by one onto these locations at a rate equal to the setted clock signal.

Results:-

ADC:-



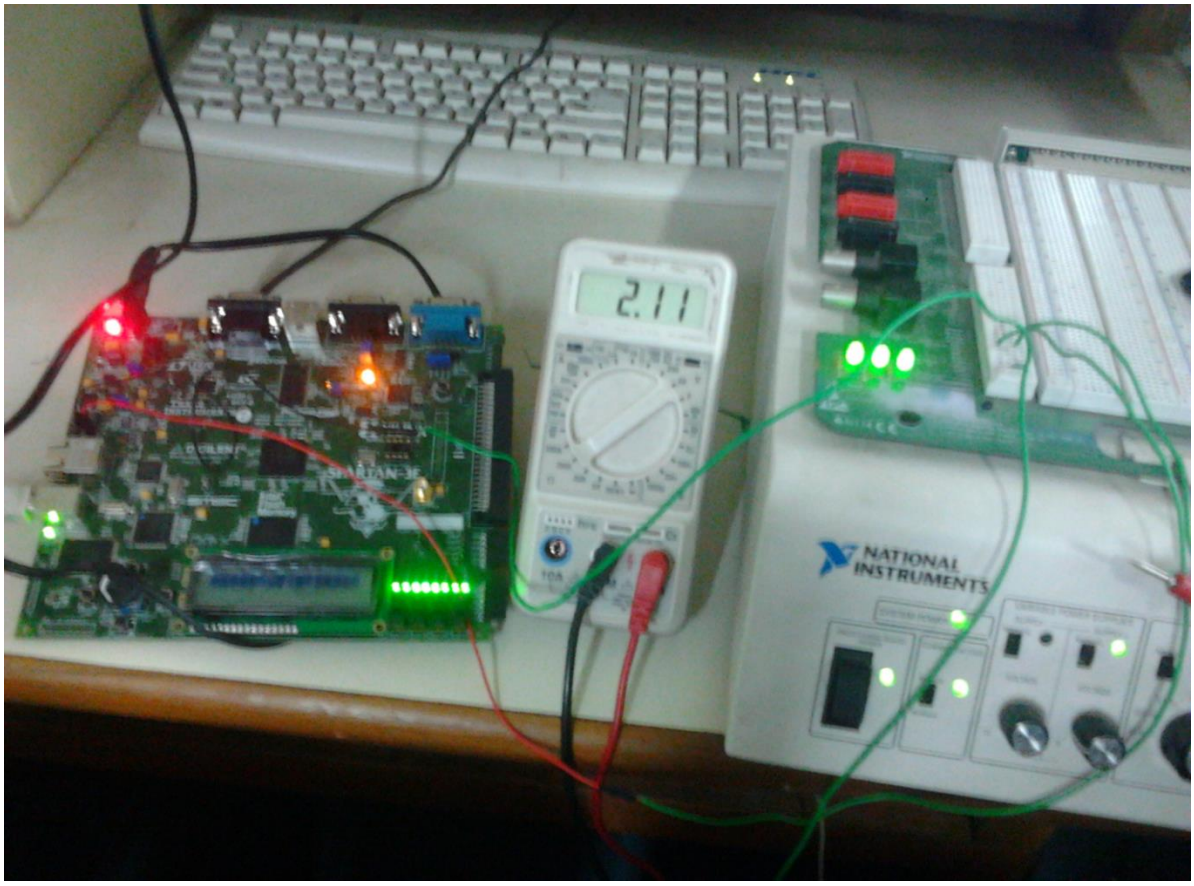
(ADC output in chip scope pro)



(ADC output in hardware)

Here, we have seen that the output coming in the chipscope pro 11000011 is same as the output in hardware. In this case we are showing only the MSBs of the 14-bit data because of shortage of LEDs.

Our input range for ADC is 0.4 to 2.9, but because of some instrumental error in the multimetre we are getting a little deviated output.



(Output for the predicted height)

Similarly here we are manually applying the Analog input from an adjustable DC source and getting corresponding digital output on the FPGA board. According to theory we should get the observed digital output at a minimum Analog voltage of 2.7V but the slight deviation is due to instrumental error in the millimeter. We can set the threshold value and by comparing this with the predicted height we can get the signal for occurrence of tsunami.

Conclusion:-

Successfully developed the pressure sensor based tsunami detection system which partially fulfils the requirements for laboratory scale studies. The response obtained in this system clearly demonstrates the usefulness of the detection system for real-time deployment.

Summary & Future enhancement:-

Overall, the result indicates the ability for an evolution of a system which can detect Tsunami in advance based on the pressure changes under the sea. If, it is being practically implemented with the future enhancement any natural disaster can be detected in advance without producing false alarms. Existing system has all the facilities to detect Tsunami. Obviously it will detect Tsunami before sometimes which are going to occur by raising an alarm. But, the problem with the existing system is, that there is a chance to produce false alarms often which threatens our government and public. So, in future Tsunami occurrence can be decided and alarm can be raised only after checking many criteria. Four criteria to be checked out before giving the tsunami alarm are as follows:

• Pressure inside the sea bed.

• Tide level.

• Biological changes in the marine living organisms.

• Sea shore level.

If all these four criteria get detected then it can be concluded that there is some occurrence of natural disaster (Tsunami).